Technical Area: ASIC Applications: Digital Signal Processing

Digital Filter ASIC for NASA Deep Space Radio Science Receiver

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Abstract

This paper is about the implementation of an 80 MHz, 16-bit, multi-stage digital filter to decimate by 1600, providing a 50 kHz output with bandpass ripple of less than +/- 0.1 dB. The chip uses two decimation by five units and six decimations by two executed by a single decimation by two unit. The six decimations by two consist of six halfband filters, five having 30-taps and one having 51-taps. Use of a 16x16 register file for the digital delay lines enables implementation in the Vitesse 350K gate array.

Summary

A Gallium Arsenide gate may was chosen to implement the digital signal processing function of decimation by 1600. The 80 MHz input signal's sampling rate is decreased by 1600 by means of eight finite impulse response (FIR) filters. The 50 kHz output has bandpass ripple of less than +/- 0.1 dB. The implementataion uses two decimation by five units and a single decimation by two unit that executes six decimations by two in series, the last having 51 taps. For speed and density, the design is implemented in a Vitesse 350K GaAs gate array.

Parallel Decimation by 5/4

The first decimation by five filter has 30 taps. Three multiplications execute in parallel, accumulating over five cycles. An additional multiplier is incorporated to allow the option of decimation by four with 32 taps.

Sequential Decimation by 5/4

The second decimation unit uses a single multiplier for identical operations as the first stage. Parallelism is not required because of the slower data rate.

Decimate by 2 Engine

The third stage is similar to the second, except that it emulates six filters, five 19-tap decimation by two, and one 51-tap decimation by two. A single add-multipy-accumulate engine is able to execute all of these operations in conjunction with an input queue consisting of a four-stage FIFO. Register files hold the data delay lines and accumulator registers for the five concurrently active accumulations. Pipelining has been used to facilitate the data processing, and pointers are used to implement the data

delay registers in register files. Due to the symetricity of the algorithm, only hal the nominal number of storage positions for the data delay registers arc needed. Since for each filter there arc only two operation sequences, depending upon whether its an even or odcl input to the filter, only two control registers arc necessary, one indicating which filter is active (a six bit shift register), and the other indicates which is the mode for each filter, even or odd.

Application

This filter will bc used in conjunction with NASA Deep Space Network Block V Digital Receiver to extract scientific information from spacecraft transmissions, e.g., when the signal travels through a planetary atmosphere. This requires linear phase, low amplitude ripple low pass filtering. The narrow output bandwidth, relative to the input 80 MHz sampling rate, allows multi-stage filtering/decimation to bc done, enabling a function that would require hundreds of taps to bc implemented in multiple filter stages, all with tap lengths of less than 52.

Contributions

The contributions to the art include, novel use of compute] structures for digital signal processing and a simple, algorithmically tailored control structure. Judicious usc of parallelism and high speed sequential operation allows relatively long filter tap lengths to bc implemented with a small number of multipliers.

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Summaries and Proposals due:	**March 3, 199S**
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Final Camera Ready Manuscript clue:	June 2, 1995

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